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| 09/558,787 | 04/26/2000 | Yuriko Kishitaka | SONYJP3.0-114 | 1701 |
| 530 | 7590 | 07/08/2004 | EXAMINER | |
| LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK 600 SOUTH AVENUE WEST WESTFIELD, NJ 07090 | | | LONSBERRY, HUNTER B | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2611 | 16 |

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/558,787

Applicant(s)

KISHITAKA ET AL.

Examiner

Hunter B. Lonsberry

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6/16/04.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-7 and 10-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-7 and 10-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-7, and 10-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,892,508 to Howe in view of U.S. Patent 5,978,855 to Metz, U.S. Patent 5,684,791 to Raychaudhuri and U.S. Patent 6,212,632 to Surine.

Regarding claims 1, 6, 7 and 12, Howe discloses a set top box 100 in figure 8 which receives an analog or digital video signal, a digital tuner 1218 supplies a digital video signal to video decoder 1220, CPU 1228 manages and controls set top box 100 and is connected to memory 1229 and 1230 (column 20, line 46-column 22, line 52).

Howe does not disclose determining an optimal buffer size that depends on a streams bitrate or having a buffer size determined after a power on signal is issued, but does disclose the use of ATM and MPEG 2 for video transmission (column 9, lines 7-65).

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Metz discloses in Figure 6, a Set top box 100, which receives MPEG 2 video encapsulated in ATM cells that encapsulated by ATM multiplexer 29, an ATM demux and MPEG system demux 127 within the STB 100 reassembles the MPEG video/audio prior to it being supplied to audio decoder 131 and video decoder 129 (column 16, line 48-column 17, line 16, column 32, lines 4-31). Metz inherently includes a buffer, as a buffer is required to store the ATM cells prior to reassembling the cells into MPEG 2 streams.

Therefore it would have been obvious to one skilled in the art at the time of invention to modify Howe to transmit MPEG 2 video encapsulated in ATM cells which is converted back into MPEG 2 video at the Set Top Box as taught by Metz thus providing more bandwidth for each channel.

Metz fails to disclose a buffer sizing scheme in response to a power on signal.

Raychaudhuri discloses a data link control layer in which buffer size is determined by the bit rate for the transmitted ATM stream (column 7, line 35-column 8, line 3).

Therefore it would have been obvious to one skilled in the art at the time of invention to modify Howe and Metz to include the ATM buffer size bit rate determination as taught by Raychaudhuri, thus insuring that a buffer would not underflow/overflow resulting in the improper display of a video image.

Raychaudhuri fails to disclose performing the buffer size determination after a power on signal is issued.

Surine discloses a buffer function, which is loaded from ROM and then is setup within an embedded computer system's RAM for allocating buffer memory upon the powering up of the device (figures 8, 9, column 4, lines 46-column 6, line 2, column 7, lines 45-57, column 8, line 65-column 9, line 21). Surine inherently detects a power up signal, as Surine discloses in Figure 8 and 9, that the boot code from the ROM is executed after power up steps 801 and 901.

Therefore, it would have been obvious to one skilled in the art at the time of invention to modify the combination of Howe, Metz and Raychaudhuri to load up a buffer program upon device startup as taught by Surine, thus enabling a device to receive and process data as soon as possible.

Regarding claims 4, 5, 10, and 11, Howe discloses the use of non-volatile memory 1214 for storing information (column 21, lines 1-29). Howe does not disclose storing the buffer size-determining program in non-volatile memory, but does disclose memory 1229 and 1230 for storing system software (column 22, lines 11-29).

Surine discloses a buffer function, which is loaded from ROM and then is setup within an embedded computer system's RAM for allocating buffer memory upon the powering up of the device (figures 8, 9, column 4, lines 46-column 6, line 2, column 7, lines 45-57, column 8, line 65-column 9, line 21).

Regarding claims 13 and 15, Howe discloses a set top box 100 in figure 8 which receives an analog or digital video signal, a digital tuner 1218 supplies a digital video signal to video decoder 1220, CPU 1228 manages and controls set

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top box 100 and is connected to memory 1229 and 1230 (column 20, line 46-column 22, line 52).

Howe does not disclose determining an optimal buffer size that depends on a streams bitrate or having a buffer size determined after a power reset signal is issued, but does disclose the use of ATM and MPEG 2 for video transmission (column 9, lines 7-65).

Metz discloses in Figure 6, a Set top box 100, which receives MPEG 2 video encapsulated in ATM cells that encapsulated by ATM multiplexer 29, an ATM demux and MPEG system demux 127 within the STB 100 reassembles the MPEG video/audio prior to it being supplied to audio decoder 131 and video decoder 129 (column 16, line 48-column 17, line 16, column 32, lines 4-31). Metz inherently includes a buffer, as a buffer is required to store the ATM cells prior to reassembling the cells into MPEG 2 streams.

Therefore it would have been obvious to one skilled in the art at the time of invention to modify Howe to transmit MPEG 2 video encapsulated in ATM cells which is converted back into MPEG 2 video at the Set Top Box as taught by Metz thus providing more bandwidth for each channel.

Metz fails to disclose a buffer sizing scheme in response to a power-reset signal.

Raychaudhuri discloses a data link control layer in which buffer size is determined by the bit rate for the transmitted ATM stream (column 7, line 35-column 8, line 3).

Therefore it would have been obvious to one skilled in the art at the time of invention to modify Howe and Metz to include the ATM buffer size bit rate determination as taught by Raychaudhuri, thus insuring that a buffer would not underflow/overflow resulting in the improper display of a video image.

Raychaudhuri fails to disclose performing the buffer size determination after a power reset signal is issued.

The examiner takes official notice that the use of a power-reset signal to reinitialize settings is well known in the art, for example, a reset button on a personal computer.

Surine discloses a buffer function, which is loaded from ROM and then is setup within an embedded computer system's RAM for allocating buffer memory upon the powering up of the device (figures 8, 9, column 4, lines 46-column 6, line 2, column 7, lines 45-57, column 8, line 65-column 9, line 21). Surine inherently detects a power up signal, as Surine discloses in Figure 8 and 9, that the boot code from the ROM is executed after power up steps 801 and 901.

Therefore, it would have been obvious to one skilled in the art at the time of invention to modify the combination of Howe, Metz and Raychaudhuri to enable a reset signal to reinitialize settings and load up a buffer program upon device startup as taught by Surine, thus enabling a device to receive and process data as soon as possible, and clear and allocated memory.

Regarding claim 14, Howe discloses a set top box 100 in figure 8, which receives an analog or digital video signal. Metz discloses a STB 100, which converts, received ATM cells back into their original MPEG 2 streams.

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Raychaudhuri discloses that the buffer size determination is made as part of the Data link Control layer in a wireless ATM system. Raychaudhuri's DLC layer is inherently part of a program to be executed by the processor as the DLC layer is part of the header file for a packet and programming is required in order to recognize that layer. Raychaudhuri inherently executes the buffer sizing program when the power is turned on as Raychaudhuri detects the type of data being received and allocates the buffer sized based upon the bit rate, if Raychaudhuri did not check that function and received various streams of different bit rates, the buffer would over/underflow.

Regarding claims 16-23, Surine discloses a buffer function, which is loaded from ROM and then is setup within an embedded computer system's RAM for allocating buffer memory upon the powering up of the device (figures 8, 9, column 4, lines 46-column 6, line 2, column 7, lines 45-57, column 8, line 65-column 9, line 21). Surine inherently detects a power up signal, as Surine discloses in Figure 8 and 9, that the boot code from the ROM is executed after power up steps 801 and 901.

Howe, Metz, Surine and Raychaudhuri do not disclose the use of a power reset, or a switch for a user to turn on the power to the device.

The examiner takes official notice that a user pressing a power on and a power reset button, which transmits a power on signal, is well known in the art.

Therefore it would have been obvious to one skilled in the art at the time of invention to modify the combination of Howe, Metz, Surine and Raychaudhuri to utilize a power on and power reset button, thus enabling a user to turn on a

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device at any time of their choosing, and allowing a user to reset a receiver if the receiver crashes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,222,592 to Patel: TV Receiver Equalizer Storing Channel Characterizations for Each TV Channel Between Times of Reception Therefrom.

U.S. Patent 6,124,878 to Adams: Optimum Bandwidth Utilization in a Shared Cable System Data Channel.

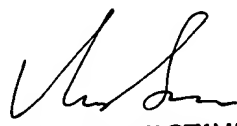
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hunter B. Lonsberry whose telephone number is 703-305-3234. The examiner can normally be reached on Monday-Friday during normal business hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Faile can be reached on 703-305-4380. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HBL



VIVEK SRIVASTAVA
PRIMARY EXAMINER